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| 10/628,237 | 07/29/2003 | Makoto Shizukuishi | 107317-00060 | 4755 |

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| EXAMINER | |
|---|---|
| TRAN, NHAN T | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2622 | |

DATE MAILED: 11/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/628,237 | SHIZUKUISHI, MAKOTO | |
| | Examiner | Art Unit | |
| | Nhan T. Tran | 2622 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *29 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 July 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Priority*

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

### *Drawings*

2. **Figure 9** should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### *Claim Objections*

3. Claims 2 & 3 are objected to because of the following informalities: both claims 2 & 3 recites "said non-volatile memory **record** the digital image data..." which should be corrected as -- said non-volatile memory **records** the digital image data ... --. Appropriate correction is required.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-8, 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morris et al. (US 6,573,936 B2) in view of Tran et al. (US 6,282,145 B1).

Regarding claim 1, Morris et al. (hereafter referred as "Morris") discloses a solid state image pickup device (Fig. 1; col. 1, lines 39-46 and col. 2, lines 16-33) comprising:

a semiconductor substrate (chip substrate) defining a two-dimensional surface (Fig. 1 and col. 1, lines 39-46 and col. 2, lines 10-16);

a number of photoelectric conversion elements (pixel sensors) disposed in a light receiving area (pixel array area 104 shown in Fig. 1) of said semiconductor substrate in a matrix shape (two dimensional matrix shape) and in a plurality of rows and columns (see col. 2, lines 16-33);

signal processors (array of A/D converters 120 shown in Fig. 1), each formed for each column of said photoelectric conversion elements in an area (area 120) of said semiconductor substrate other than the light receiving area (col. 2, lines 53-58, wherein area 120 is clearly formed at a different area of the chip substrate from the pixel array area 104), said signal processor at least converting analog image data from said photoelectric conversion elements into digital image data (see col. 2, lines 53-65);

a memory (a memory array 130) formed in correspondence with respective photoelectric conversion elements in an area (area 130) of said semiconductor substrate other than the light receiving area at a succeeding stage of said signal processor (see Fig. 1 in which the memory array area 130 is clearly formed at a different area of the chip substrate from the pixel array area 104), said memory recording the digital image data (see col. 1, lines 39-46 and col. 3, lines 3-10).

Morris teaches that the memory (130) is a random access memory (RAM), etc. (col. 3, lines 8-10). However, Morris fails to teach that the memory is a non-volatile memory.

In the same field of endeavor for processing and storing image signals in an image pickup apparatus, Tran et al. (hereafter referred as "Tran") teaches a memory improvement for storing digital images (Fig. 1D) by using a non-volatile memory (2000) to replace a conventional random access memory (RAM) because the non-volatile memory retains image data in memory cells even if the power supply is removed. This is contrast to volatile memory (RAM) which loses data if the power supply is removed (see Tran, col. 1, lines 22-35). Tran further teaches that the non-volatile memory is also preferred due to its small size with a high density array for an integrated single chip camera (integrated circuit ECAM 2005 shown in Fig. 1D) comprising an image sensor (2003), A/D converter (2002), non-volatile memory (2000) and a microcontroller (2001) (see Tran, col. 1, lines 36-41 and col. 6, lines 34-58).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the image pickup device in Morris to use a non-

volatile memory array in place of memory array 130 within the single chip image pickup device in view of the teaching of Tran so that image data is retained in the memory cells even if power supply is removed from the device (by accident or other causes) so as to prevent lost of image data during image capturing process.

Regarding claim 2, the combined teachings of Morris and Tran also discloses that the non-volatile memory records the digital image data of one frame (see Tran, col. col. 2, lines 7-17 in which the non-volatile memory has a capacity of giga bits that are inherently capable of recording one or more image frames).

Regarding claim 3, the limitations are also met by the analysis of claim 2 in which the non-volatile memory records the digital image data of a plurality of frames.

Regarding claim 4, the combined teachings of Morris and Tran also discloses erasing means (memory controller 132, 134 in Morris) for erasing the digital image data after the digital image data stored in said non-volatile memory (modified memory 130 in claim 1) is read to an external (via I/O interface 160 in Morris). See Morris, Fig. 1, col. 3, lines 10-12 & col. 7, lines 20-30 and Tran, col. 4, lines 50-54 and col. 6, lines 53-56. It should be noted that since the non-volatile memory is on-chip memory, in order to capture more new images when the memory is full with previously captured images, the previous images stored in the memory must be erased by memory controller either automatically or manually after the images are transferred to an external device via I/O

interface to yield memory space for capturing the next images for the single chip image pickup device to function as disclosed.

Regarding claim 5, Morris in view of Tran as analyzed in claim 1 also teaches that addresses of said non-volatile memory (modified memory 130 in claim 1) in a vertical direction is related to addresses of the light receiving area in the vertical direction (see Morris, Fig. 1 in which the addresses of memory 130 and pixel array 104 in a vertical direction are related in order to perform parallel processing as disclosed in col. 3, lines 3-10 and col. 7, lines 20-30).

Regarding claim 6, Morris in view of Tran as analyzed in claim 1 discloses a data register (latch B shown in Fig. 4 of Morris) used in common for both data input and output for said non-volatile memory (modified memory 130; see Morris, col. 4, lines 46-55, wherein latch B is used as data register for both reading from and writing to memory 130).

Regarding claim 7, Morris in view of Tran as analyzed in claim 1 also teaches that said non-volatile memory (modified memory 130) has a depth of same bits (8 bits) as output bits (8 bits) of said signal processor (A/D converter 120) provided for each column. See Morris, col. 3, lines 3-8 & col. 2, lines 53-58 and Tran, col. 7, lines 31-36.

Regarding claim 8, Morris in view of Tran as analyzed in claim 1 discloses that each of said signal processors (each of A/D converter 120) outputs the digital image data of one row of said photoelectric conversion elements in parallel, and said non-volatile memory (modified memory 130) records the digital image data of one row output parallel at a memory position corresponding to a row direction (array of memory 130 is arranged in a row direction to receive digital image data row by row output from the A/D converter array 120 in parallel fashion for parallel processing as disclosed by Morris, Fig. 1, col. 1, lines 10-14 and col. 3, lines 3-10).

Regarding claim 15, Morris further discloses a MOS circuit (an inherent MOS transistor in the CMOS image array 102) for reading charges from said photoelectric conversion elements in the light receiving area and transfers analog image data to said signal processor (A/D converter 120) provided for each column, and wiring lines (see Morris, Fig. 1 and col. 2, lines 29-33).

Regarding claim 16, Although Morris discloses that the solid state image pickup device works as a digital camera (Morris, col. 1, lines 39-46), Morris is silent about a shutter control unit and an optical system. However, such lack of teaching is compensated by Tran. Tran clearly teaches an integrated chip as a digital camera system (SILICONCAM 2008 shown in Fig. 1D) includes a shutter control unit (microcontroller 2001 for controlling exposure time which represents a shutter control

unit), an optical system (lens block 2004) for focusing an image of an object. See Tran, col. 6, lines 34-58.

Therefore, it would have been obvious to one of ordinary skill in the art to combine teachings of Morris and Tran to arrive at the Applicant's claimed invention by integrating a shutter control unit for controlling exposure time of the image sensor, an optical system for focusing an image of an object into the image sensor in addition to other necessary components to make a single chip digital camera to capture quality digital images while reducing size of the camera.

Regarding claim 14, Morris teaches a CMOS for reading charges from said photoelectric conversion elements in the light receiving area and transfers analog image data to said signal processor provided for each column (see the analysis of claim 15). Morris does not teach a CCD for reading charges from the photoelectric conversion elements.

As suggested by Tran, an image sensor (2003) can be either a CMOS circuit or an alternative CCD circuit for reading charges from photoelectric conversion elements (Tran, col. 6, lines 45-46).

Therefore, it would have been obvious to one of ordinary skill in the art to use a CCD in an alternative configuration for reading signal charges from the photoelectric conversion elements since the CCD is known as having an advantage in providing higher dynamic range of image signals than CMOS sensor.

5. Claims 9-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morris et al. and Tran et al. as applied to claim 1 and in further view of Yamazaki et al. (US 6,556,475 B2).

Regarding claims 9 & 10, the combination of Morris and Tran is silent about the non-volatile memory being a NAND type transistor memory (claim 9) or a NOR type transistor memory (claim 10). However, as taught by Yamazaki et al. (hereafter referred as "Yamazaki"), it is well recognized in the art that non-volatile memory can be made with a NAND type transistor memory, a NOR type transistor memory, etc. (Yamazaki, col. 1, lines 40-49). Regardless the types, the non-volatile memory is highly desired for storing data in various electronic devices for substituting volatile memory such as DRAM (Yamazaki, col. 1, lines 32-40).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to configure the non-volatile memory in Morris and Tran with a NAND type transistor memory or an alternative NOR type transistor memory for storing image data in view of the teaching of Yamazaki because both types have a common advantage of retaining image data in memory cells even if the power supply is removed and are highly desirable for storing data in electronic devices while providing more choices and flexibility to designer for making different image pickup models based on different types of transistor memories toward different camera applications and consumers.

Regarding claims 11 & 12, the combination of Morris, Tran and Yamazaki further discloses that the transistor memory has a floating gate type memory structure, MONOS type memory structure (see Yamazaki, col. 1, lines 40-49).

Regarding claim 13, the combination of Morris, Tran and Yamazaki also discloses that the transistor memory is a ferroelectric memory (see Tran, col. 4, lines 30-42).

***Conclusion***

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nhan T. Tran whose telephone number is (571) 272-7371. The examiner can normally be reached on Monday - Friday, 8:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

NT

NHAN T. TRAN
Patent Examiner